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09/927,675	08/10/2001	Guy Perry	MTI-31471	6524

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EXAMINER	
CHU, CHRIS C	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,675	PERRY, GUY	
	Examiner	Art Unit	
	Chris C. Chu	2815	MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 34, 50 - 65 and 69 - 70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 34, 50 - 65 and 69 - 70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's response filed on October 16, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 5, 7 - 14, 16 - 19, 21 - 24, 26 - 34, 50 - 53, 55, 57 - 65 and 69 - 76 are rejected under 35 U.S.C. 102(b) as being anticipated by Preslar et al. '643.

Regarding claim 1, Preslar et al. discloses in e.g., Fig. 3 and Fig. 4 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (40 and 40a) and second bond pad (42 and 42a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads.

Regarding claims 2 and 17, Preslar et al. discloses in e.g., Fig. 4, and column 6, lines 18 - 52 the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer (material) between the first and second bond pads to a substrate underlying the bond pads.

Regarding claim 5, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 further comprising a conductive material (52, at the joint portion of the wire) interconnecting the first bond pad to the second bond pad.

Regarding claim 7, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 the conductive material (52, at the joint portion of the wire) overlies at least a portion of each of the first and second bond pads.

Regarding claim 8, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 further comprising a bonding wire (the terminal wire) connected to the conductive material.

Regarding claim 9, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 6, lines 18 - 52 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads;
- wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

Regarding claim 10, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 - 32 further comprising a conductive material (52, at the joint portion of the wire) interconnecting and overlying at least a portion of the first and second bond pads.

Regarding claim 11, Preslar et al. discloses in e.g., Fig. 3 and Fig. 4 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of the first bond pad (40 and 40a) extending beneath the upper metal layer (42) of the second bond pad (42 and 42a).

Regarding claim 12, Preslar et al. discloses in e.g., Fig. 3 and Fig. 4 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (42 and 42a) and a second bond pad (40 and 40a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of the second bond pad (40 and 40a) extending beneath the upper metal layer (42) of the first bond pad (42 and 42a).

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

Regarding claim 13, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (40 and 40a) interconnected to a second bond pad (42 and 42a) by a conductive material (52, at the joint portion of the wire);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads.

Regarding claim 14, Preslar et al. discloses in e.g., Fig. 3 and Fig. 4 the conductive material overling a portion of each of the bond pads.

Regarding claims 16 and 21, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 further comprising a bonding wire (the terminal wire) connected to the conductive material.

Regarding claim 18, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a) positioned within a single passivation opening (under 36);
- the first and second bond pads interconnected by a conductive material (52, at the joint portion of the wire) overlying at least a portion of each of the bond pads; and
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads.

Regarding claim 19, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 7, lines 22 – 26 a passivation layer (the passivation layer) overlying a portion of each of the bond pads, the opening (at the place of 36) being through the passivation layer to expose the bond pads.

Regarding claim 22, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first metal layer (40a and 42a) deposited onto a substrate (72) and patterned to form first (40a) and second (42a) lower metal layer portions having a space thereinbetween;
- a dielectric layer (a material in 66 and 66a) deposited over the first and second lower metal layer portions and the substrate within the space (66a), and etched to form openings (66) to each of the first and second lower metal layer portions; and
- a second metal layer (40 and 42) deposited over the dielectric layer and into the openings of the dielectric layer and etched to form a first (40) and second (42) upper metal layer portions overlying and in conductive contact with the first and second lower metal layer portions;
- the first upper (40) and lower (40a) metal layer portions forming a first bond pad, and the second upper (42) and lower (42a) metal layer portions forming a second bond pad;
- wherein a lower metal layer (40a) portion of one (40 and 40a) of the bond pads extends beneath the upper metal layer (42) portion of the other (42 and 42a) of the bond pads.

Regarding claim 23, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 7, lines 22 – 26 a passivation layer (the passivation layer) formed over the bond pads and etched to form an opening (at the place of 36) therethrough to expose the first and second bond pads.

Regarding claim 24, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 further comprising a conductive material (52, at the joint portion of the wire) interconnecting the first bond pad to the second bond pad.

Regarding claim 26, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 the conductive material overlies at least a portion of each of the first and second bond pads.

Regarding claim 27, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 further comprising a bonding wire (the terminal wire) connected to the conductive material.

Regarding claim 28, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (42 and 42a) and a second bond pad (40 and 40a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending beneath the upper metal layer (42) of the other (42 and 42a) of the bond pads; and
- at least one of the bond pads functions to supply data, test a device, or supply various voltage levels.

Regarding claim 29, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 the first bond pad (42 and 42a) being functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the

second bond pad, the first and second bond pads are functional to a receive and respond to operational mode signals.

Regarding claim 30, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending beneath the upper metal layer (42) of the other (42 and 42a) of the bond pads; and
- at least one of the bond pads functions to supply data, test a device, or supply various voltage levels;
- the first bond pad (40 and 40a) being functional to receive and respond to a test mode signal (at the place of 50) by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to a receive and respond to operational mode signals; and
- the lower metal layer (40a) of the first bond pad (40 and 40a) extending beneath or underneath the upper metal layer (42) of the second bond pad (42 and 42a).

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

Regarding claim 31, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 the lower metal layer (40a) of the second bond pad (40 and 40a) extending beneath or underneath the upper metal layer (42) of the first bond pad (42 and 42a).

Regarding claims 32 and 34, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (42 and 42a) and a second bond pad (40 and 40a);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads; and
- the first bond pad (42 and 42a) functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads functional to a receive and respond to an operational mode signals by entering an operational mode; and
- the lower metal layer (40a) of the second bond pad (40 and 40a) extending beneath or underneath the upper metal layer (42) of the first bond pad (42 and 42a).

Regarding claim 33, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) in a semiconductor device (6a), comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads; and

- the first bond pad (40 and 40a) functional to receive and respond to a test mode signal (at the place of 50) by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads functional to a receive and respond to an operational mode signals by entering an operational mode; and
- the lower metal layer (40a) of the first bond pad (40 and 40a) extending beneath or underneath the upper metal layer (42) of the second bond pad (42 and 42a).

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

Regarding claims 50 and 51, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 an integrated circuit die (6a), comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a), the first and second bond pads being positioned within a single passivation (the passivation layer) opening (at the place of 36);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads.
- the lower metal layer (40a) of the first bond pad (40 and 40a) extending underneath the upper metal layer (42) of the second bond pad (42 and 42a).

Regarding claim 52, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 an integrated circuit die (6a), comprising:

- a first bond pad (42 and 42a) and a second bond pad (40 and 40a), the first and second bond pads being positioned within a single passivation (the passivation layer) opening (at the place of 36);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending underneath the upper metal layer (42) of the other (42 and 42a) of the bond pads; and
- the lower metal layer (40a) of the second bond pad (40 and 40a) extending underneath the upper metal layer (42) of the first bond pad (42 and 42a).

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

Regarding claim 53, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a conductive material (52, at the joint portion of the wire) interconnecting and overlying at least a portion of the first bond pad and the second bond pad.

Regarding claim 55, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bonding wire (the terminal wire) connected to at least one of the bond pads.

Regarding claim 57, Preslar et al. discloses in e.g., Fig. 4, and column 6, lines 18 - 52 the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

Regarding claim 58, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 - 52 an integrated circuit die, comprising:

- a first bond pad (40 and 40a) interconnected to a second bond pad (42 and 42a), the first and second bond pads being positioned within a single passivation (the passivation layer) opening (at the place of 36);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (40a) of one (40 and 40a) of the bond pads extending beneath the upper metal layer (42) of the other (42 and 42a) of the bond pads;
- wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

Regarding claim 59, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 the first and second bond pads being interconnected by a conductive material (52, at the joint portion of the wire) interconnecting overlying and in conductive contact with at least a portion of each of the bond pads.

Regarding claim 60, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 - 52 an integrated circuit die (6a), comprising:

- a first bond pad (40 and 40a) interconnected to a second bond pad (42 and 42a), the first and second bond pads being positioned within a single passivation (the passivation layer) opening (at the place of 36);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; and

- the lower metal layer (40a) of the first bond pad extending beneath the upper metal layer (42) of the second bond pad.

Regarding claim 61, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 - 52 an integrated circuit die (6a), comprising:

- a first bond pad (42 and 42a) interconnected to a second bond pad (40 and 40a), the first and second bond pads being positioned within a single passivation (the passivation layer) opening (at the place of 36);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- with the lower metal layer (40a) of the second bond pad extending beneath the upper metal layer (42) of the first bond pad.

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

Regarding claim 62, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 - 52 an integrated circuit die (6a), comprising:

- a first bond pad (42 and 42a) and a second bond pad (40 and 40a);
- each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer;
- the lower metal layer (40a) of one (40 and 40a) of the bond pads extending beneath the upper metal layer (42) of the other (42 and 42a) of the bond pads; and
- at least one of the bond pads functional to supply data, retrieve data, test a device, or supply various voltages.

Further, terms such as "first" and "second" are merely relative terms, which do not patternably distinguish claimed structure over Preslar et al.

Regarding claims 63 and 65, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a conductive material (52, at the joint portion of the wire) interconnecting and overlying at least a portion of each of the bond pads.

Regarding claim 64, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 the first bond pad (42 and 42a) being functional to receive and respond to a test mode signal by entering a test mode, and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to receive and respond to an operational mode signal by entering an operational mode.

Regarding claim 69, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) disposed on a substrate (72) and comprising multiple bond pads (40 & 40a and 42 & 42a), each bond pad comprising overlying upper and lower metal layers, and the upper metal layer (42) of one (42 and 42a) of the bond pads overlapping the lower metal layer (40a) of another (40 and 40a) of the bond pads.

Regarding claim 70, Preslar et al. discloses in e.g., Fig. 3, Fig. 4 and column 5, lines 28 – 32 a bond pad structure (36) disposed on a substrate (72) and comprising two or more bond pads (40 & 40a and 42 & 42a), each bond pad comprising overlying upper and lower metal layers, and the upper metal layer (42) of one (42 and 42a) of the bond pads extending over the lower metal layer (40a) of another (40 and 40a) of the bond pads.

Regarding claim 71, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 a bond pad structure (36) disposed on a substrate (72) and comprising:

- a lower metal layer (40a and 42a) disposed on the substrate (72) and comprising first (40a) and second (42a) portions separated by a space (66a) therebetween;
- a dielectric layer (the layer 66 and 66a) overlying the lower metal layer and the substrate within the space;
- one or more openings (66a) extending through the dielectric layer to each of the first and second lower metal portions; and
- an upper metal layer (40 and 42) disposed over the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer;
- the upper metal layer comprising first (40) and second (42) portions, the first upper metal portion (40) positioned over the first lower metal portion (40a) to form a first bond pad, and the second upper metal portion (42) positioned over the second lower metal portion (42a) to form a second bond pad; and
- the upper metal portion (42) of one (42 and 42a) of the bond pads extends over the lower metal portion (40a) of the other (40 and 40a) bond pad.

Regarding claim 72, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 - 52 an integrated circuit supported by a substrate and comprising:

a bond pad structure (36), the bond pad structure comprising two or more bond pads (40 & 40a and 42 & 42a), each bond pad comprising overlying upper and lower metal layers,

and the upper metal layer (42) of one (42 and 42a) of the bond pads extending over the lower metal layer (40a) of another (40 and 40a) of the bond pads.

Regarding claim 73, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 an integrated circuit supported by a substrate and comprising:

- a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and
- the upper metal layer (42) of one (42 and 42a) of the bond pads extends beyond the lower metal layer (42a) of the one bond pad and over the lower metal layer (40a) of the other (40 and 40a) of the bond pads.

Regarding claim 74, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 an integrated circuit supported by a substrate and comprising a bond pad structure (36), the bond pad structure comprising:

- a lower metal layer (40a and 42a) comprising first (40a) and second (42a) portions with a space (66a) therebetween;
- a dielectric layer (the layer in 66 and 66a) overlying the lower metal layer and within the space;
- at least one opening extending through the dielectric layer to each of the first and second lower metal portions; and
- an upper metal layer (40 and 42) overlying the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer;

- the upper metal layer (40 and 42) comprising first (40) and second (42) portions, the first upper metal portion (40) positioned over the first lower metal portion (40a) to form a first bond pad, and the second upper metal portion (42) positioned over the second lower metal portion (42a) to form a second bond pad; and
- the upper metal portion (42) of one (42 and 42a) of the bond pads extends over the lower metal portion (40a) of the other bond pad (40 and 40a).

Regarding claim 75, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 a semiconductor device (6a), comprising:

- a substrate (72); and
- a bond pad structure (36) disposed on the substrate (72), the bond pad structure comprising multiple bond pads (40 & 40a and 42 & 42a), each bond pad comprising overlying upper and lower metal layers, and the upper metal layer (42) of one of the bond pads (42 and 42a) overlaps the lower metal layer (40a) of another (40 and 40a) of the bond pads.

Regarding claim 76, Preslar et al. discloses in e.g., Fig. 3, Fig. 4, column 5, lines 28 – 32 and column 6, lines 18 – 52 a semiconductor wafer, comprising:

- a substrate (72) and a bond pad structure (36) disposed on the substrate, the bond pad structure comprising a first bond pad (40 and 40a) and a second bond pad (42 and 42a);
- each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and

- the upper metal layer (42) of one (42 and 42a) of the bond pads extends beyond the lower metal layer (42a) of the one bond pad and over the lower metal layer (40a) of the other (40 and 40a) of the bond pads.

4. Claims 1 – 4 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Muramatsu et al. '664.

Regarding claim 1, Muramatsu et al. discloses in e.g., Fig. 1 and Fig. 18 a bond pad structure (26) in a semiconductor device (10), comprising:

- a first bond pad (A and B) and second bond pad (D and E);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (B and/or C) of one of the bond pads extending underneath the upper metal layer (D) of the other of the bond pads.

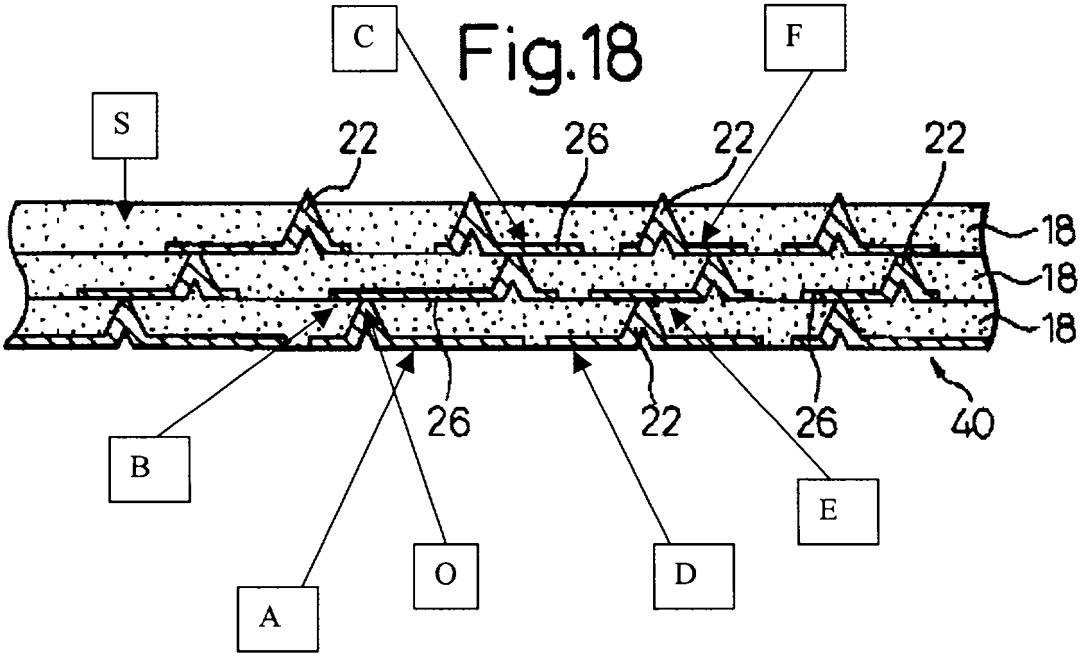

Fig.18

Regarding claims 2 and 17, Muramatsu et al. discloses in e.g., Fig. 1 and Fig. 18 the extension of the lower metal layer (B) of the one of the bond pads functions as an etch block (at the place of O) to prevent etching of a dielectric layer (material 18) between the first and second bond pads to a substrate (S) underlying the bond pads.

Regarding claim 3, Muramatsu et al. discloses in e.g., Fig. 1 and Fig. 18 at least one (B) of the lower metal layers (B and C) of the one of the bond pads (A - C) extends underneath the upper metal layer (D) of the other of the bond pads (D - F).

Regarding claim 4, Muramatsu et al. discloses in e.g., Fig. 1 and Fig. 18 at least two lower metal layers (B and C) of the one of the bond pads (A - C) extend underneath the upper metal layer (D) of the other of the bond pads (D - F).

Regarding claim 9, Muramatsu et al. discloses in e.g., Fig. 1 and Fig. 18 a bond pad structure (26) in a semiconductor device (10), comprising:

- a first bond pad (A and B) and a second bond pad (D and E);
- each of the bond pads comprising at least a lower metal layer and an upper metal layer;
- with a lower metal layer (B) of one (A and B) of the bond pads extending underneath the upper metal layer (D) of the other (D and E) of the bond pads;
- wherein the extension of the lower metal layer (B) of the one (A and B) of the bond pads functions as an etch block (at the place of O) to prevent etching of a dielectric layer (material 18) between the first and second bond pads to a substrate (S) underlying the bond pads.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 15, 20, 25 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Preslar et al. in view of Geffken et al. '435.

Preslar et al. discloses the claimed invention except for the conductive material comprising a solder material or solder. However, Geffken et al. teaches in Fig. 7 and column 5, lines 13 – 25 a conductive material (174) comprising a solder material or solder. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by using the solder material or solder for the conductive material as taught by Geffken et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of increasing the bond strength between the pads and the external device (e.g., wire).

7. Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over Preslar et al. in view of Muramatsu et al.

Regarding claim 56, Preslar et al. does not disclose the first and second bond pads each comprising a plurality of lower metal layers wherein at least two lower metal layers of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads. Muramatsu

et al. teaches in e.g., Fig. 1 and Fig. 18 a first (A - C) and second (D - F) bond pads each comprising a plurality of lower metal layers wherein at least two lower metal layers (B and C) of the one (A – C) of the bond pads extend underneath an upper metal layer (D) of the other (D - F) of the bond pads. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Preslar et al. by using the plurality of lower metal layers with at least two lower metal layers as taught by Muramatsu et al. The ordinary artisan would have been motivated to modify Preslar et al. in the manner described above for at least the purpose of providing a predetermined electrical connection pattern (column 14, lines 34 and 35).

Response to Arguments

8. Applicant's arguments with respect to claims 1 – 34, 50 – 65 and 69 - 76 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hively and Maitani et al. disclose the pad structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
12/31/03 10:51:07 PM

B.WILLIAM BAUMEISTER
PRIMARY EXAMINER